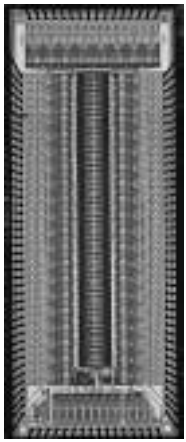
STV7620M

PLASMA DISPLAY PANEL DATA DRIVER

FEATURES

- 96 Outputs Plasma Display Driver
- 95V Absolute Maximum Rating
- Reduced EMI (Electro Magnetic Interference)
- 3.3V/5V Compatible Logic
- -40/30mA Source / Sink Output Mos
- 3 or 6 Bit Data Bus (40MHz)
- BCD Process
- Packaging Adapted to Customer Request (DICE, COB, COF, TAB).



DIE ORDER CODE: STV7620M/WAF(1)

(1) tested wafer

Please contact STMicroelectronics for ordering information concerning samples or bump version

DESCRIPTION

STV7620M is a data driver for Plasma Display Panels (PDPs) designed in the ST's proprietary BCD high voltage technology. A new shape of the output pulse generated by the STV7620M ensures a noticeable EMI reduction. Using a 3 or 6 bit wide data bus, the STV7620M can control 96 high current, high voltage outputs. The STV7620M is supplied by a separate 80V for the power outputs and 5V for the logic. All command inputs are CMOS and 3.3V logic level compatible.

Revision follow-up

Target specification

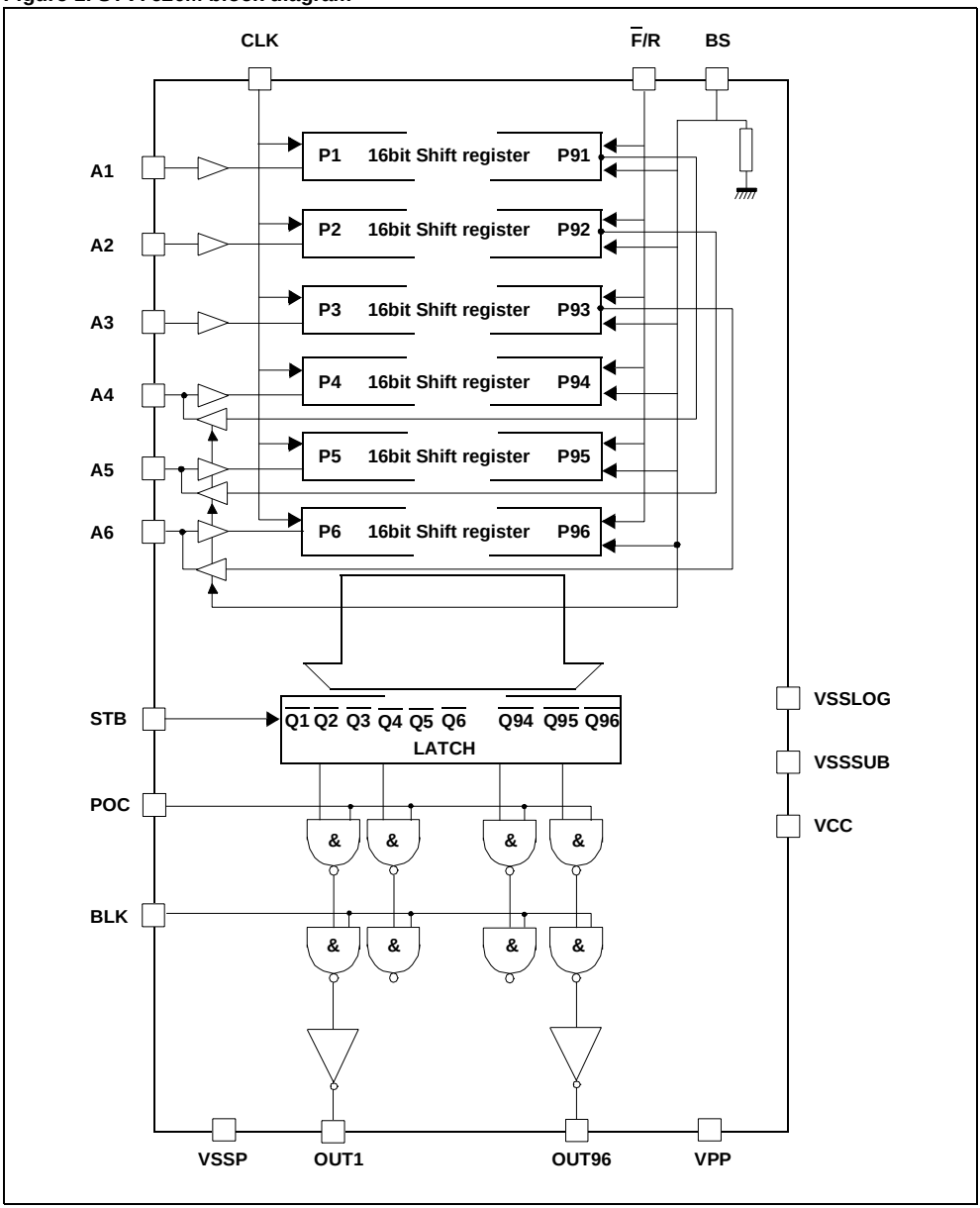
02/2001	version 1.0
	document creation
03/2001	version 1.1
	general update, addition of EMI and figure 1
04/2001	version 1.2
	general update, new pads dimensions
10/2001	version 1.3
	addition of die photo in cover page, new pads dimensions
	Electrical characteristics: replaced a few TBD mentions with values
	AC timing characteristics: some TBD replaced with values
	F/$\overline{R}$ replaced with $\overline{F}$/R
	Electrical characteristics: Idoutl/h value replaced with ±30mA

Preliminary data

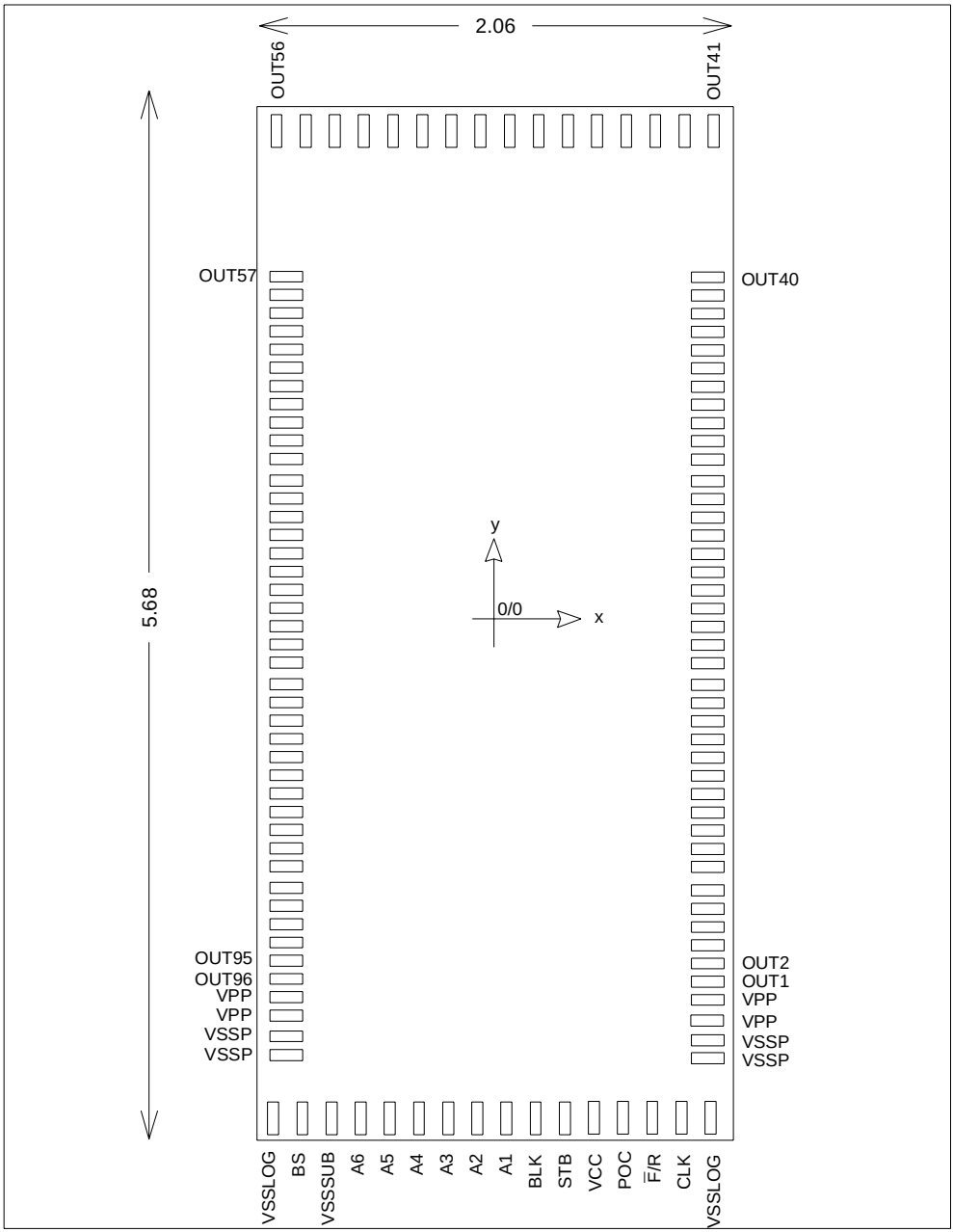
02/2002	version 3.0
	whole document: sales type becomes STV7620M for slow, medium, fast general update
04/02/2002	version 3.1
	general update
05/22/2002	version 3.2
	issued from version 3.0 Addition of input/output schematics
04/2003	version 3.3
	sales type changed to STV7620M general updates
04/2003	version 3.4
	general updates
05/2003	version 3.5
	Page 1, Description paragraph, power output supply changed to 80V.
10/2003	version 3.6
	added section 4 BUMP DIMENSIONS on page 7
26 Feb. 2004	version 3.7
	Page 11: Icc changed from 100 to 15µA and Ipph from 100 to 10µA

1 BLOCK DIAGRAM

Figure 1. STV7620M block diagram



2 DIE PIN OUT / DIE DESCRIPTION



3 PADS DIMENSIONS (in μm)/ PADS POSITIONS

The reference is the centre of the die (x=0, y=0)
Pad size is specified for wire-bonding options

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TOP SIDE from left to right

Name	Centre:X	Centre:Y	Size:x	SIze: y
OUT56	-773.670	2695.987	76.330	102.425
OUT55	-670.480	2695.987	76.330	102.425
OUT54	-567.290	2695.987	76.330	102.425
OUT53	-464.100	2695.987	76.330	102.425
OUT52	-360.910	2695.987	76.330	102.425
OUT51	-257.720	2695.987	76.330	102.425
OUT50	-154.530	2695.987	76.330	102.425
OUT49	-51.340	2695.987	76.330	102.425
OUT48	51.850	2695.987	76.330	102.425
OUT47	155.040	2695.987	76.330	102.425
OUT46	258.230	2695.987	76.330	102.425
OUT45	361.420	2695.987	76.330	102.425
OUT44	464.610	2695.987	76.330	102.425
OUT43	567.800	2695.987	76.330	102.425
OUT42	669.460	2695.987	76.330	102.425
OUT41	772.650	2695.987	76.330	102.425

BOTTOM SIDE from right to left

Name	Centre:X	Centre:Y	Size:x	SIze: y
Vsslog	771.630	-2695.988	76.330	102.425
Clk	669.545	-2695.988	76.330	102.425
F/R	566.355	-2695.988	76.330	102.425
Pol	463.165	-2695.988	76.330	102.425
Vcc	359.975	-2695.988	76.330	102.425
Stb	257.635	-2695.988	76.330	102.425
Blk	154.445	-2695.988	76.330	102.425
A1	51.255	-2695.988	76.330	102.425
A2	-51.935	-2695.988	76.330	102.425
A3	-155.125	-2695.988	76.330	102.425
A4	-258.315	-2695.988	76.330	102.425
A5	-361.505	-2695.988	76.330	102.425
A6	-464.695	-2695.988	76.330	102.425

BOTTOM SIDE from right to left

Name	Centre:X	Centre:Y	Size:x	SIze: y
Vsssub	-567.885	-2695.988	76.330	102.425
BS	-669.545	-2695.988	76.330	102.425
Vsslog	-771.630	-2695.988	76.330	102.425

RIGHT SIDE from top to bottom

Name	Centre:X	Centre:Y	Size:x	SIze: y
OUT40	887.612	1949.985	102.425	76.330
OUT39	887.612	1846.795	102.425	76.330
OUT38	887.612	1745.135	102.425	76.330
OUT37	887.612	1641.945	102.425	76.330
OUT36	887.612	1538.755	102.425	76.330
OUT34	887.612	1332.375	102.425	76.330
OUT33	887.612	1229.185	102.425	76.330
OUT32	887.612	1125.995	102.425	76.330
OUT31	887.612	1022.805	102.425	76.330
OUT30	887.612	919.615	102.425	76.330
OUT29	887.612	816.425	102.425	76.330
OUT28	887.612	713.235	102.425	76.330
OUT27	887.612	610.045	102.425	76.330
OUT26	887.612	506.855	102.425	76.330
OUT25	887.612	403.665	102.425	76.330
OUT24	887.612	300.475	102.425	76.330
OUT23	887.612	197.285	102.425	76.330
OUT22	887.612	94.095	102.425	76.330
OUT21	887.612	-9.095	102.425	76.330
OUT20	887.612	-112.285	102.425	76.330
OUT19	887.612	-215.475	102.425	76.330
OUT18	887.612	-318.665	102.425	76.330
OUT17	887.612	-421.855	102.425	76.330
OUT16	887.612	-525.045	102.425	76.330
OUT15	887.612	-628.235	102.425	76.330
OUT14	887.612	-731.425	102.425	76.330

RIGHT SIDE from top to bottom

Name	Centre:X	Centre:Y	Size:x	SIze: y
OUT13	887.612	-834.615	102.425	76.330
OUT12	887.612	-937.805	102.425	76.330
OUT11	887.612	-1040.995	102.425	76.330
OUT10	887.612	-1144.185	102.425	76.330
OUT9	887.612	-1247.375	102.425	76.330
OUT8	887.612	-1350.565	102.425	76.330
OUT7	887.612	-1453.755	102.425	76.330
OUT6	887.612	-1556.945	102.425	76.330
OUT5	887.612	-1660.135	102.425	76.330
OUT4	887.612	-1763.325	102.425	76.330
OUT3	887.612	-1866.515	102.425	76.330
OUT2	887.612	-1969.705	102.425	76.330
OUT1	887.612	-2072.895	102.425	76.330
Vpp	887.612	-2175.915	102.425	76.330
Vpp	887.612	-2279.105	102.425	76.330
Vssp	887.612	-2382.210	102.425	76.330
Vssp	887.612	-2485.400	102.425	76.330

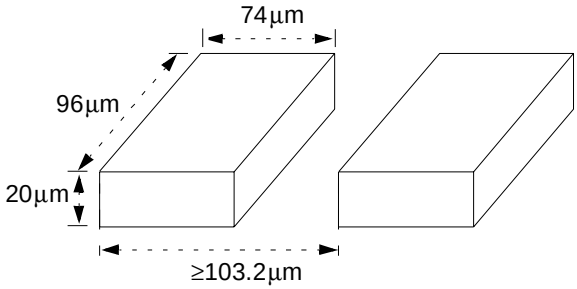
LEFT SIDE from bottom to top

Name	Centre:X	Centre:Y	Size:x	SIze: y
Vssp	-887.612	-2485.400	102.425	76.330
Vssp	-887.612	-2382.210	102.425	76.330
Vpp	-887.612	-2279.105	102.425	76.330
Vpp	-887.612	-2175.915	102.425	76.330
OUT96	-887.612	-2072.895	102.425	76.330
OUT95	-887.612	-1969.705	102.425	76.330
OUT94	-887.612	-1866.515	102.425	76.330
OUT93	-887.612	-1763.325	102.425	76.330
OUT92	-887.612	-1660.135	102.425	76.330
OUT91	-887.612	-1556.945	102.425	76.330
OUT90	-887.612	-1453.755	102.425	76.330
OUT89	-887.612	-1350.565	102.425	76.330
OUT88	-887.612	-1247.375	102.425	76.330
OUT87	-887.612	-1144.185	102.425	76.330
OUT86	-887.612	-1040.995	102.425	76.330
OUT85	-887.612	-937.805	102.425	76.330

LEFT SIDE from bottom to top

Name	Centre:X	Centre:Y	Size:x	SIze: y
OUT84	-887.612	-834.615	102.425	76.330
OUT83	-887.612	-731.425	102.425	76.330
OUT82	-887.612	-628.235	102.425	76.330
OUT81	-887.612	-525.045	102.425	76.330
OUT80	-887.612	-421.855	102.425	76.330
OUT79	-887.612	-318.665	102.425	76.330
OUT78	-887.612	-215.475	102.425	76.330
OUT77	-887.612	-112.285	102.425	76.330
OUT77	-887.612	-9.095	102.425	76.330
OUT75	-887.612	94.095	102.425	76.330
OUT74	-887.612	197.285	102.425	76.330
OUT73	-887.612	300.475	102.425	76.330
OUT72	-887.612	403.665	102.425	76.330
OUT71	-887.612	506.855	102.425	76.330
OUT70	-887.612	610.045	102.425	76.330
OUT69	-887.612	713.235	102.425	76.330
OUT68	-887.612	816.425	102.425	76.330
OUT67	-887.612	919.615	102.425	76.330
OUT66	-887.612	1022.805	102.425	76.330
OUT65	-887.612	1125.995	102.425	76.330
OUT64	-887.612	1229.185	102.425	76.330
OUT63	-887.612	1332.375	102.425	76.330
OUT62	-887.612	1435.565	102.425	76.330
OUT61	-887.612	1538.755	102.425	76.330
OUT60	-887.612	1641.945	102.425	76.330
OUT59	-887.612	1745.135	102.425	76.330
OUT58	-887.612	1846.795	102.425	76.330
OUT57	-887.612	1949.985	102.425	76.330

4 BUMP DIMENSIONS



Bump composition: gold

5 DATA BUS CONFIGURATION

BS	F/R	Input	Data Shift														
			CLK	01	02	03	04	05	06	...	11	12	13	14	15	16	
L	L	A1	Out	01	07	13	19	25	31		61	67	73	79	85	91	Forward Shift
		A2	Out	02	08	14	20	26	32		62	68	74	80	86	92	
		A3	Out	03	09	15	21	27	33		63	69	75	81	87	93	
		A4	Out	04	10	16	22	28	34		64	70	76	82	88	94	
		A5	Out	05	11	17	23	29	35		65	71	77	83	89	95	
		A6	Out	06	12	18	24	30	36		66	72	78	84	90	96	
L	H	A1	Out	91	85	79	73	67	61		31	25	19	13	07	01	Reverse Shift
		A2	Out	92	86	80	74	68	62		32	26	20	14	08	02	
		A3	Out	93	87	81	75	69	63		33	27	21	15	09	03	
		A4	Out	94	88	82	76	70	64		34	28	22	16	10	04	
		A5	Out	95	89	83	77	71	65		35	29	23	17	11	05	
		A6	Out	96	90	84	78	72	66		36	30	24	18	12	06	
			CLK	01	02	03	04	05	06	...	27	28	29	30	31	32	
H	L	A1	Out	01	04	07	10	13	16		79	82	85	88	91	94	Forward
		A2	Out	02	05	08	11	14	17		80	83	86	89	92	95	
		A3	Out	03	06	09	12	15	18		81	84	87	90	93	96	
H	H	A1	Out	94	91	88	85	82	79		16	13	10	07	04	01	Reverse
		A2	Out	95	92	89	86	83	80		17	14	11	08	05	02	
		A3	Out	96	93	90	87	84	81		18	15	12	09	06	03	

This table describes the position of the first data sampled by the first rising edge of the CLK signal. For the first configuration described in the above table, (BS = “L” and F/R= “L”), data on A1 bus sampled by the 1st clock pulse is applied on Output1. After 16 clock pulses this data will be shifted to Output 91.

6 PIN DESCRIPTION

Symbol	Function	Description
OUT(01-96)	Output	Power output
VSSP	Ground	Ground of power outputs
VPP	Supply	High voltage supply of power outputs
BLK	Input	Blanking input
POC	Input	Power output control input
$\overline{F}$/R	Input	Selection of shift direction
BS	Input	Selection of 3/6 bits shift register
VCC	Supply	5V logic supply
VSSLOG	Ground	Logic ground
VSSSUB	Ground	Substrate ground
CLK	Input	Clock of data shift register
STB	Input	Latch of data to outputs
IN (A1-A6)	Input	Shift register input for BS = “L”
IN (A1-A3)	Input	Shift register input for BS = “H”
OUT(A4-A6)	output	A1, A2, A3 shift register output for BS=”H”

7 CIRCUIT DESCRIPTION

STV7620M includes all the logic and power circuits necessary to drive column electrodes of a Plasma Display Panel (P. D. P.). Binary values of each pixel of the displayed line are loaded into the shift register by a 6 bit wide (A1 - A6) or 3 bit wide (A1 - A3) data bus, depending on the configuration of the BS input pin. Data is shifted at each low-to-high transition of the CLK clock.

The forward/reverse ($\overline{F}$/R) input is used to select the direction of the shift register.

The BS input sets the configuration of the shift register either in 3 x 32 bits or in 6 x 16 bits.

In case of a 3 bit arrangement, A1, A2 and A3 data bus input pins are used. The 3 shift registers are loaded with 32 clock pulses. A4, A5 and A6 data bus pins are the outputs of A1, A2 and A3 shift registers respectively.

The maximum frequency of the shift clock is 40MHz. This leads to an equivalent 240MHz serial shift register for a 6 x 16 bits arrangement.

When the STB signal is Low, data are transferred from the shift register to the latch and the power output stages.

All the output data are kept memorised and held in the latch stage when the latch input STB is pulled high.

Vsssub and Vsslog must be connected as close as possible to the logical reference ground of the application.

STV7620M is supplied with a 5 volt power supply. All the logic inputs can be driven either by 5V CMOS logic or by 3.3V CMOS logic.

A low EMI function has been implemented: the falling edge of the outputs has 2 slopes, a smooth one for 30ns followed by a steeper one.

Table 1: Shift register truth table

	Input		Shift register function
BS	$\overline{F}$/R	CLK	Output Q
X	L	rise	Forward shift
X	L	H or L	Steady
X	H	rise	Reverse shift
X	H	H or L	Steady
H	X	X	3 bits shift register
L	X	X	6 bits shift register

Table 2: Power output truth table

Pn	STB	BLK	POC	Driver Output	Comments
X	X	L	X	all L	Output at low level
X	X	H	L	all H	Output at high level
X	H	H	H	Qn	Data latched
L	L	H	H	L	Data copied
H	L	H	H	H	Data copied

Pn+1 = A1, Pn+2 = A2, Pn+3 = A3, Pn+4 = A4, Pn+5 = A5, Pn+6 = A6, n = [0,6,12,18,...,90] and BS = “L”

8 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vcc	Logic supply range	-0.3, +7	V
Vpp	Driver supply range	-0.3, +95	V
Vin	Logic input voltage range	-0.3, Vcc+0.3	V
Ipout	Driver output current (Note 1)(Note 3) (Note 4)	- 40 / +30	mA
I_{dout}	Diode Output Current (Note 2) (Note 3) (Note 4)	-200 / +300	mA
Tjmax	Maximum junction temperature	125	°C
Tstg	Storage temperature range	-50, +150	°C
Vout	Output power voltage range	-0.3, +90	V

Note 1: Through one power output.

Note 2: Through one power output for all power outputs (see Figure 4) with junction temperature lower than or equal to Tjmax

Note 3: These parameters are measured during ST's internal qualification which includes temperature characterisation on standard batches and on corners batches of the process. These parameters are not tested on the parts.

Note 4: Transient current. Spike current duration inferior to 300ns.

Caution: in accordance with the Absolute Maximum Rating System (IEC 60134), product quality may suffer if the maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum rating are not exceeded.

9 ELECTRICAL CHARACTERISTICS

(Vcc = 5V, Vpp = 70V, Vssp = 0V, Vss = 0V, Tamb = 25°C, FCLK = 40MHz, unless otherwise specified)

Symbol	Parameter	Min.	Typ	Max	Unit
SUPPLY					
Vcc	Logic supply voltage	4.50	5	5.5	V
Icc	Logic supply current (Note 5)	-		15	µA
Iccl	Logic Dynamic Supply Current (FCLK= 20Mhz) (Note 6)	-	20	-	mA
Icc	Logic Supply Current (Vih= 2.0V)		500	750	µA
Vpp	Power output supply voltage	15		80	V
Ipph	Power output supply current (steady outputs)	-	-	10	µA
OUTPUT					
OUT1-OUT96					
Vpouth	Power output high level (voltage drop versus Vpp) @Ipouth = - 20mA and Vpp = 70V	-	7.5	14	V
Vpoutl	Power output low level @ Ipoutl = + 20mA	-	5	11	V
Vdouth	Output diode voltage drop @ Idouth = + 30mA (Note 7)	-	1	2	V
Vdoutl	Output diode voltage drop @ Idoutl = - 30mA (Note 7)	-2	-1	-	V
INPUT					
CLK, $\overline{F}$/R, STB, POC, BLK, BS, A1-A6					
Vih	Input high level	2.0	-	-	V
Vil	Input low level	-	-	0.9	V
Iih	High level input current (Vih≥2.0V)	-	-	5	µA
Iil	Low level input current (Vil = 0V)	-	-	5	µA
Iih	High level input current for BS (Vih = 5V)		20		µA
Cin	Input capacitance			15	pF
A4-A6					
Voh	Logic output high level (Ioh = -1mA)		4.85		V
Vol	Logic output low level (Iol = 1mA)		0.1		V

Note 5: Logic input levels compatible with 5V CMOS logic
Note 6: All data inputs are commuted at 10MHz
Note 7: see Figure 4.Test configuration page15

10 AC TIMING REQUIREMENTS

(Vcc = 4.5V to 5.5V, T amb = -20 to +85°C, input signals max leading edge & trailing edge (tr,tf) = 5ns)

Symbol	Parameter	Min.	Typ	Max	Unit
t_{CLK}	Data clock period	25	-	-	ns
t_{WHCLK}	Duration of CLK pulse at high level	10	-	-	ns
t_{WLCLK}	Duration of CLK pulse at low level	10	-	-	ns
t_{SDAT}	Set-up time of data input before low to high clock transition	5	-	-	ns
t_{HDAT}	Hold-time of data input after low to high clock transition	5	-	-	ns
t_{HSTB}	Hold-time of STB after low to high clock transition	5	-	-	ns
t_{STB}	STB low level pulse duration	10	-	-	ns
t_{SSTB}	STB set-up time before CLK rise	5			ns

11 AC TIMING CHARACTERISTICS

(Vcc = 5V, Vpp = 70V, Vssp = 0V, Vsssub = 0V, Vsslog = 0V, Tamb = 25°C, FCLK = 40MHz,)
(Vilmax = 0.2Vcc, Vihmin = 0.8Vcc)

Symbol	Parameter	Min.	Typ	Max	Unit
t_{PHL1} t_{PLH1}	Delay of power output change after CLK transition - high to low - low to high	 - -	 35 30	 100 100	 ns ns
t_{PHL2} t_{PLH2}	Delay of power output change after STB transition - high to low - low to high	 -	 - -	 95 95	 ns ns
t_{PHL3} t_{PLH3}	Delay of power output change after BLK, POC transition - high to low - low to high	 -	 25 20	 90 90	 ns ns
$t_{R\ OUT}$	Power output rise time (Note 8)	50	-	200	ns
$t_{F\ OUT}$	Power output fall time (Note 8)	50	-	200	ns
t_S	Width of the falling edge smooth shape (not tested)	-	30	-	ns
$t_{R\ DAT}$	Logic data output rise time (CL = 10pF)	-	9	20	ns
$t_{F\ DAT}$	Logic data output fall time (CL = 10pF)	-	5	12	ns
t_{PHL4} t_{PLH4}	Delay of logic data output change after CLK transition - high to low - low to high	 - -	 12 13	 25 25	 ns ns

Note 8: one output among 96, loading capacitor CL = 50pF, other outputs at low level

Figure 2. AC Characteristics Waveform

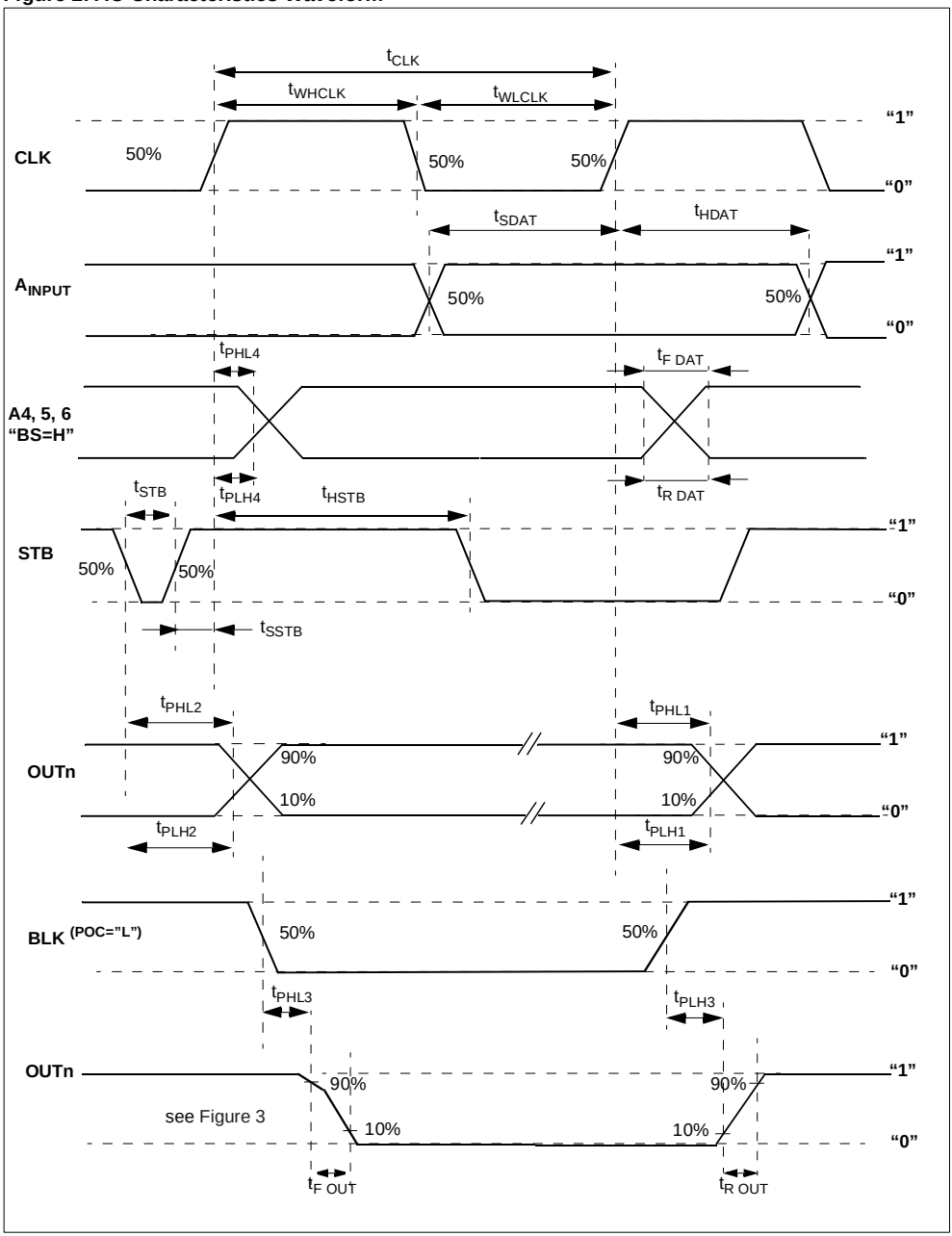


Figure 3. Zoom for OUTn showing t_S and $t_{F\ OUT}$

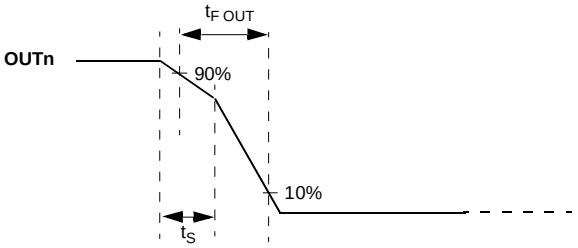
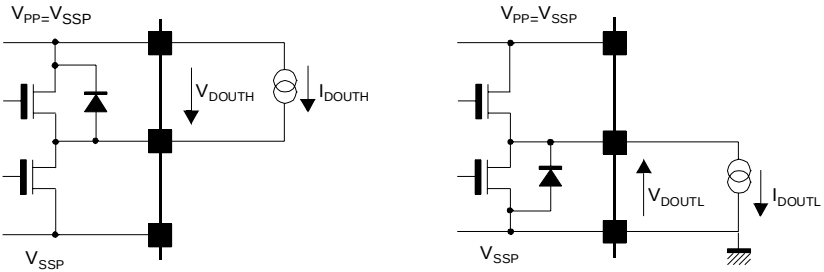


Figure 4. Test configuration



Output sinking current as positive value, sourcing current as negative value

12 - INPUT/OUTPUT SCHEMATICS

Figure 5. B/S input

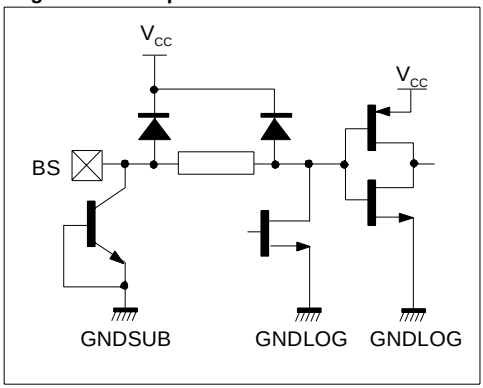


Figure 6. A4 to A6

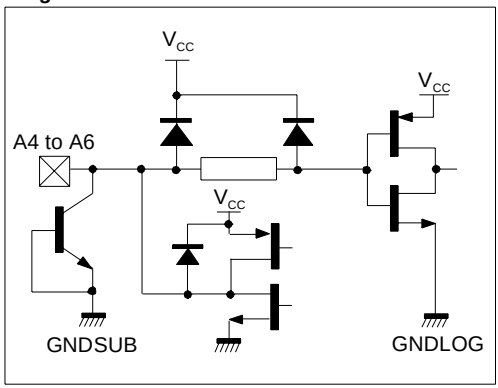


Figure 7. CLK, STB, r/R, POC, BLK, A1 to A3 inputs

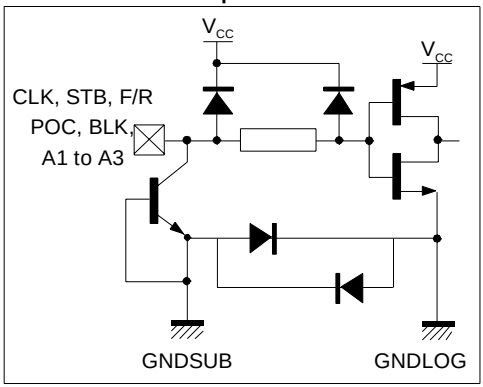


Figure 8. Power output